REMARKS

Claims 1-13 and 15-22 remain pending in the current Application. Claim 3 has been amended to include a semicolon after "memory" in line 3. No other amendments to the claims have been made herein. Applicants submit that the amendments do not add new matter to the current Application. All the amendments herein have been made in order to clarify the claims and not for prior art reasons. Applicants also submit that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Claim Rejections under 35 U.S.C. 102 and 103(a)

Claims 1 – 2 and 21

Applicants respectfully submit that claims 1 - 2 and 21 are patentable under 35 U.S.C. 103(a) over US Patent No. 6,275,926 (hereinafter referred to as Samra) in view of US Patent No. 5,594,765 (hereinafter referred to as Oh), and over Hennessy in view of US Patent No. 4,541,045 (hereinafter referred to as Kromer). With respect to claim 1, Applicants submit that Samra and Oh, alone or in combination, do not teach or suggest each and every element of claim 1. For example, claim 1 includes an address bus for providing a current address and a previous address and means for generating a first sequence signal that when negated indicates the current address may not be sequential to the previous address, a second sequence signal that when negated indicates that the current address is not sequential to the previous address, and a third sequence signal that when negated indicates that the current address, if it is an instruction address, is not sequential to the previous address that was an instruction address. That is, note that each of the first, second, and third signals, when negated, are used to provide information regarding the sequentialness of *the current address*. That is, the current address is introduced as "a current address" in the first element of claim 1, and each subsequent element of claim 1 refers to "the

current address," which indicates that it is the same current address as introduced in the first element of claim 1. Samra, Oh, nor their combination teach, suggest, or provide motivation to generate the first, second, and third sequence signals as claimed in claim 1.

For example, the Examiner states that Oh's LATCH signal teaches the first sequence signal of claim 1 because it indicates that the current address may not be sequential to the previous address. Therefore, the Examiner has denoted that the latched address (the beginning address of a burst) is the current address, and the fact that LATCH was asserted to bring in a beginning address, this address may not be sequential to the previous address. The Examiner then proceeds to state that Oh's "seq_int#" signal teaches the second sequence signal because it specifies either sequential or interleaved burst mode. The Examiner states that when negated and thus in interleaved mode, "the current address *will be* non-sequential with respect to the previous address" (emphasis added). That is, as acknowledged by the Examiner, the seq_int# signal indicates that the counting scheme *will be* interleaved, thus providing an indication of the relation of a subsequent address to a current address but provides no indication of the relation of the current address to the previous one. The Examiner has already denoted that the current address corresponds to the beginning of the burst cycle, since the Examiner states that LATCH is the first sequence signal. Therefore, the seq_int# signal does not indicate a relation of this current address (i.e. the beginning address of the burst cycle) to a previous address, but instead indicates a relation of a subsequent address to a current one (e.g. the relation of the second burst address with respect to the beginning burst address). However, claim 1 claims that the first sequence signal, when negated, indicates *the current address* may not be sequential to *the previous address*, and the second sequence signal, when negated, indicates *the current address* is not sequential to the *previous address*. That is, both the first and second sequence signals provide an indication as to the sequentialness of the same current address. Therefore, the Examiner cannot assume one current address for the first sequence signal (i.e. .the beginning address of a burst) and assume a different current address for the second sequence signal (the address that *will be* the current address at some time later based on seq_int#). In the Examiner's Response Arguments section, page 27, paragraph b, the Examiner argues that the relationship of a subsequent address to a current address is the same as the relationship of a current address and a previous address, and states that "therefore, this signal [seq_int#] does provide an indication of the relationship between a current and previous address ...." However, it does not indicate the

relationship of the same current address and previous address as the LATCH signal. Therefore, the LATCH signal *and* seq_int# signals of Oh are not provided as sequence signals for a current address. For at least these reasons, Applicants submit that claim 1 is allowable over Samra in view of Oh.

Still referring to claim 1, Applicants (in their previous response) stated that the negation of the seq_int# does not necessarily indicate that two addresses are not sequential because sequential addresses do exist in Oh's interleaved schemes. In the response to arguments section of the current Office Action, the Examiner states that the Applicant does not claim that the signal (i.e. the second sequence signal) "**definitely** indicates that the current address is not sequential to the previous address." However, the claim 1 states "a second sequence signal that when negated indicates that the current address *is not* sequential to the previous address." The term "is not sequential" means *is not sequential*, i.e. definitely not sequential, and cannot be interpreted to mean "it may or may not be sequential." Therefore, the second sequence signal of claim 1, when negated, indicates that the current address is not sequential to the previous address. However, one cannot rely upon the negation of the seq_int# signal to indicate that an address will be non-sequential, because even in interleaved mode, sequential addresses occur. Therefore, for these additional reasons, Applicants submit that claim 1 is allowable over Samra in view of Oh.

Also, still referring to claim 1, the Examiner states that in Samra, if it is determined that the branch direction was mispredicted, then a third signal must inherently exist which indicates that a misprediction has occurred. Again, the third sequence signal of claim 1, when negated, indicates *the current address*, if is an instruction address, is not sequential to the previous address that was an instruction address. That is, the third sequence signal is also provided with respect to the current address. Firstly, a branch misprediction signal is not generated to indicate that a current address is not sequential to a previous one, but instead, to indicate that a different address needs to fetched to correct the branch misprediction. For example, at the time this "inherent" misprediction signal is generated to indicate that the previous prediction was wrong, and the system, in response to this misprediction, will subsequently fetch (at the next cycle, or at some other later cycle) a new address which may or may not be sequential. However, this new address is *not* the current address, it is a subsequent address. Furthermore, there would be no motivation to use a branch misprediction signal for the beginning address of a burst (which the Examiner has denoted as the "current address"). That is, the LATCH indicates the start of a

burst and there is no motivation to also generate a branch misprediction signal at the start of a burst. Therefore, for at these additional reasons, Applicants submit that claim 1 is allowable over Samra in view of Oh.

Applicants also respectfully submit that claim 1 is patentable over Hennessy in view of Kromer, as introduced in the Examiner's new rejections in the current Office Action. Hennessy, Kromer, nor their combination teach or suggest all the elements of claim 1. The Examiner states that Hennessy's branch prediction scheme teaches the first and second sequence signals. For example, the Examiner states that the branch prediction is the first sequence signal in that it indicates if a current address may be sequential to a previous address and states that the second sequence signal is the one which represents the actual outcome of the branch. However, this signal occurs with respect to a later address, i.e. when the branch instruction is actually resolved; therefore, it does not indicate that *the current address* is not sequential to the previous one. That is, it is no longer the current address (the current address when the branch prediction was made), but it is a subsequent address. However, as discussed above, claim 1 claims generating the first *and* second sequence signal with respect to the current address. Therefore, the Examiner cannot denote one current address for the first sequence signal and then change which address is denoted as the current address for the second sequence signal.

Furthermore, with respect to the first sequence signal and Hennessy, the Examiner states that the branch prediction indicates that the current address may be sequential to a previous address and provides the example that, "if a branch is predicted taken, then the current address may not be sequential to the previous address. It may not be sequential because it is merely a prediction and the actual address is not known yet." However, Applicants respectfully submit that the Examiner has mischaracterized the reference. Regardless of how a branch is predicted, the next address fetched is known and it will either *be* sequential or non-sequential, depending on if the branch is predicted taken or not. That is, even though the actual address is not yet known (and therefore, the prediction may have been wrong), instructions are continuously fetched in a known manner (i.e. a known sequence) until the branch is resolved and the actual address is known. Therefore, there are addresses fetched between the branch prediction and the time at which the actual address is known. Therefore, as stated above, the branch prediction signal and the branch resolution signal (resulting in the knowledge of the actual address) do not teach or suggest a first sequence signal that, when negated, indicates *the current address* may not be

sequential to the previous address and a second sequence signal that, when negated, indicates *the current address* is not sequential to the previous address (where the current address referred to with respect to the second sequence signal is the same as the current address referred to with respect to the first sequence signal, since both refer to "*the current address*").

Still referring to claim 1 with respect to Hennessy in view of Kromer, the Examiner states that the VALID + .5 signal of Kromer teaches a third sequence signal that when negated indicates that the current address, if it is an instruction address, is not sequential to the previous address that was an instruction address. However, Applicants respectfully disagree. Referring to FIG. 2C of Kromer, VALID + .5 is negated for I_4, i.e. the current address, which clearly *is* sequential to the previous instruction address, I_3. Therefore, when negated, VALID +.5 does not indicate that the current address is not sequential to the previous address that was an instruction address. Furthermore, the Examiner states on page 13 of the current Office Action that "for as long as the instruction addresses are sequential, signal VALID+.5 (FIG. 2C) remains high." However, this is not true. For example, in FIG. 2C, VALID+.5 is high, yet I_N (the branch target instruction) is not sequential to I_5. Also, the Examiner cites col. 7, lines 58, to col. 8, line 18, and states that "the VALID+.5 signal goes low when the branch destination (80) is encountered, in this case for instruction I_4." However, as disclosed in col. 8, lines 4–8, of Kromer, the VALID+.5 signal goes low indicative of the fact that I_4, the jump address, is not a valid instruction, i.e., not an instruction requiring decoding. That is, unlike the Examiner's assertions, the VALID+.5 signal is used to indicate when an instruction is a valid instruction needing decoding or not and does not indicate whether a branch has been encountered or not. Therefore, I_4, which in this example represents a jump address, is only one example of an invalid instruction (i.e. one that is not to be decoded), as denoted by VALID + .5. Furthermore, the branch is not actually encountered until I_N, at which point VALID+.5 remains high. Therefore, for at least these reasons, Kromer does not teach or suggest a third sequence signal as claimed in claim 1.

Furthermore, none of the cited references provide any motivation for generating multiple signals with respect to a same current address. For example, claim 1 claims the first sequence signal, when negated, indicates that the current address may not be sequential to the previous address and the second signal, when negated, indicates that the current address is not sequential to the previous address. None of the cited references, alone or in combination, provide motivation for having two signals generated with respect to the current and previous address,

where one is used to indicate whether the current address may not be sequential to the previous address and one used to indicate whether the current address is not sequential to the previous address. None of the cited references, including Oh, Samra, Kromer, and Hennessy, provide any motivation for the use of multiple signals, such as the first and second sequence signals.

With respect to claim 2, claim 2 further claims that if the current address is not sequential to the previous address, the first sequence signal is negated prior to the second sequence signal being negated. Claim 2 depends from allowable claim 1 and is therefore at least allowable over the cited references for at least those reasons provided with respect to claim 1. However, Applicants submit that none of the cited references teach or suggest the limitations of claim 2 either. The Examiner states that, with respect to Samra in view of Oh, "it should be noted that in order to be in sequential or interleaved burst mode, the system must first be in a general burst mode. Therefore, the first signal (LATCH) will provide an indication before the second signal (seq_int#)." However, the use of the LATCH does not indicate that the system is in a general burst mode, but instead, it specifically latches a beginning burst address, thus indicating the beginning of a burst cycle. Therefore, upon beginning a burst cycle, the system of Oh already needs to know in which mode to operate, interleaved or sequential (as indicated by seq_int#). Therefore, seq_int# must be set prior to initiating a burst cycle. Therefore, for these additional reasons, Applicants submit that claim 2 is allowable over Samra in view of Oh.

Claims 2-3 have not been independently addressed because they depend directly or indirectly from allowable claim 1 and are therefore also allowable for at least those reasons provided above with respect to claim 1.

Claims 3 - 9

Applicants respectfully submit that claims 3-9 are patentable over Samra in view of Oh and over Hennessy in view of Kromer. With respect to claim 3, Applicants submit that Samra and Oh, alone or in combination, do not teach or suggest each and every element of claim 3. For example, claim 3 includes an address bus for providing a current address and a previous address and means for generating a first sequence signal that when negated indicates the current address may not be sequential to the previous address, a second sequence signal that when negated indicates that the current address is not sequential to the previous address, and a third sequence

signal that when negated indicates that the current address, if it is an instruction address, is not sequential to the previous address that was an instruction address. That is, note that each of the first, second, and third signals, when negated, are used to provide information regarding the sequentialness of *the current address*. That is, the current address is introduced as "a current address" in the first element of claim 3, and each subsequent element of claim 3 refers to "the current address," which indicates that it is the same current address as introduced in the first element of claim 3. As discussed above with respect to claim 1, Samra, Oh, nor their combination teach, suggest, or provide motivation to generate multiple sequence signals corresponding to a relationship of a current address and a previous address. Similarly, as also discussed above with respect to claim 1, Hennessy, Kromer, nor their combination teach, suggest, or provide motivation to generate multiple sequence signals corresponding to a relationship of a current address and a previous address. Many of the same arguments provided above with respect to claim 1 apply to claim 3; therefore, claim 3 is allowable over the cited references for at least those reasons provided above with respect to claim1.

Claims 4-9 have not been independently addressed because they depend directly or indirectly from allowable claim 3 and are therefore also allowable for at least those reasons provided above with respect to claim 3.

Claims 10-12

Applicants respectfully submit that claims 10-12 are patentable under 35 U.S.C. 102 over Kromer. With respect to claim 10, Applicants submit that Kromer does not teach or suggest each and every element of claim 10. For example, claim 10 claims an address bus for providing a current address, a previous address, and a data address wherein the data address occurs before the current address and after the previous address. Furthermore, claim 10 claims a fetch unit for generating a first sequence signal that when asserted indicates that the current address is sequential to the previous address and when negated indicates that the current address may not be sequential to the previous address. Kromer does not teach or suggest these elements.

With respect to claim 10, the Examiner states that the VALID + .5 signal of Kromer teaches a first sequence signal that when asserted indicates that the current address is sequential to the previous address, and when negated, indicates that the current address may not be

sequential to the previous address. However, Applicants respectfully disagree. The Examiner states on that "for as long as the instruction addresses are sequential, signal VALID+.5 (FIG. 2C) remains high." However, this is not true. For example, in FIG. 2C, VALID+.5 is high, yet I_N (the branch target instruction) is not sequential to I_5. Also, the Examiner cites col. 7, lines 58, to col. 8, line 18, and states that "the VALID+.5 signal goes low when the branch destination (80) is encountered, in this case for instruction I_4." However, as disclosed in col. 8, lines 4-8, of Kromer, the VALID+.5 signal goes low indicative of the fact that I_4, the jump address, is not a valid instruction, (where only valid instructions require decoding). That is, unlike the Examiner's assertions, the VALID+.5 signal is used to indicate when an instruction is a valid instruction needing decoding or not and does not indicate whether a branch has been encountered or not. For example, the branch is not actually encountered until I_N, at which point VALID+.5 remains high. Therefore, for at least these reasons, Kromer does not teach or suggest a third sequence signal as claimed in claim 1.

Claims 11-12 have not been independently addressed because they depend directly or indirectly from allowable claim 10 and are therefore also allowable for at least those reasons provided above with respect to claim 10.

Claims 13-17 and 22

Applicants respectfully submit that claims 3-17 and 22 are patentable under 35 U.S.C. 103 over Samra in view of Oh and under 35 U.S.C. over Hennessy. With respect to claim 13, Applicants submit that Samra, Oh, and Hennessy, alone or in combination, do not teach or suggest each and every element of claim 13. For example, claim 13 claims a fetch unit for providing a first sequence signal which indicates if a current address may be sequential to a previous address and a second sequence signal which indicates if the current address is sequential to the previous address. None of the cited references, alone or in combination, teach, suggest, or provide motivation for a fetch unit which provides two signals, one indicating if a current address may be sequential to a previous address and another one indicating if the current address is sequential to the previous one.

With respect to the rejection of claim 13 over Samra in view of Oh, the Examiner states that Oh's LATCH signal teaches the first sequence signal of claim 1 because it indicates that the

current address may not be sequential to the previous address. Therefore, the Examiner has denoted that the latched address (the beginning address of a burst) is the current address, and the fact that LATCH was asserted to bring in a beginning address, this address may be sequential to the previous address. The Examiner then proceeds to state that Oh's "seq_int#" signal teaches the second sequence signal because it specifies either sequential or interleaved burst mode. The Examiner states that when asserted and thus in sequential mode, "the current address *will be* sequential with respect to the previous address" (emphasis added). That is, as acknowledged by the Examiner, the seq_int# signal indicates that the counting scheme *will be* sequential, thus providing an indication of the relation of a subsequent address to a current address but provides no indication of the relation of the current address to the previous one. The Examiner has already denoted that the current address corresponds to the beginning of the burst cycle, since the Examiner states that LATCH is the first sequence signal. Therefore, the seq_int# signal does not indicate a relation of this current address (i.e. the beginning address of the burst cycle) to a previous address, but instead indicates a relation of a subsequent address to a current one (e.g. the relation of the second burst address with respect to the beginning burst address). However, in claim 13, both the first and second sequence signals provide an indication as to the sequentialness of the same current address. Therefore, the Examiner cannot assume one current address for the first sequence signal (i.e. .the beginning address of a burst) and assume a different current address for the second sequence signal (the address that *will be* the current address at some time later based on seq_int#). In the Examiner's Response Arguments section, page 27, paragraph b, the Examiner argues that the relationship of a subsequent address to a current address is the same as the relationship of a current address and a previous address, and states that "therefore, this signal [seq_int#] does provide an indication of the relationship between a current and previous address ...." However, it does not indicate the relationship of the same current address and previous address as the LATCH signal. Therefore, the LATCH signal *and* seq_int# signals of Oh are not provided as sequence signals for a current address. For at least these reasons, Applicants submit that claim 13 is allowable over Samra in view of Oh.

Applicants also submit that claim 13 is not taught or suggested by Hennessy. The Examiner states that Hennessy's branch prediction scheme teaches the first and second sequence signals. For example, the Examiner states that the branch prediction is the first sequence signal in that it indicates if a current address may be sequential to a previous address and states that the

second sequence signal is the one which represents the actual outcome of the branch. However, this signal occurs with respect to a later address, i.e. when the branch instruction is actually resolved; therefore, it does not indicate that *the current address* is not sequential to the previous one. That is, it is no longer the current address (the current address when the branch prediction was made), but it is a subsequent address. However, as discussed above, claim 13 claims generating the first *and* second sequence signal with respect to the current address. Therefore, the Examiner cannot denote one current address for the first sequence signal and then change which address is denoted as the current address for the second sequence signal.

Furthermore, with respect to the first sequence signal, the Examiner states that the branch prediction indicates that the current address may be sequential to a previous address and provides the example that, "if a branch is predicted not taken, then the current address may be sequential to the previous address. It may be sequential because it is merely a prediction and the actual address is not known yet." However, Applicants respectfully submit that the Examiner has mischaracterized the reference. Regardless of how a branch is predicted, the next address fetched *is* known and it will either *be* sequential or non-sequential, depending on if the branch is predicted taken or not. That is, even though the actual address is not yet known (and therefore, the prediction may have been wrong), instructions are continuously fetched (in a known sequence) until the actual address is known. Therefore, there are addresses fetched between the branch prediction and the time at which the actual address is known, and the current address is therefore different for each. Therefore, as stated above, the branch prediction signal and the branch resolution signal (resulting in the knowledge of the actual address) do not teach or suggest a first sequence signal that, when negated, indicates *the current address* may not be sequential to the previous address and a second sequence signal that, when negated, indicates *the current address* is not sequential to the previous address (where the current address referred to with respect to the second sequence signal is the same as the current address referred to with respect to the first sequence signal, since both refer to "*the current address*").

Furthermore, none of the cited references provide any motivation for generating multiple signals with respect to a same current address. For example, claim 13 claims a first and second sequence signal, both providing information on a current address and a previous address. None of the cited references, alone or in combination, provide motivation for having two signals generated with respect to the current and previous address, where one is used to indicate whether

the current address may be sequential to the previous address and one used to indicate whether the current address is sequential to the previous address. None of the cited references, including Oh, Samra, Kromer, and Hennessy, provide any motivation for the use of multiple signals, such as the first and second sequence signals.

Therefore, for at least these reasons, Applicants submit that claim 13 is allowable over the cited references. Claims 14-17 and 22 have not been independently addressed because they are allowable over the cited references for at least those reasons provided above with respect to claim 13.

Claims 18-20

Applicants respectfully submit that claims 18-20 are patentable over Kromer. With respect to claim 18, Applicants submit that Kromer does not teach each and every element of claim 18. For example, claim 18 claims a fetch unit for providing a first sequence signal that indicates if a current instruction address is sequential to a previous instruction address even if a data address is provided between the current instruction address and the previous instruction address. Kromer does not teach or suggest these elements.

With respect to claim 18, the Examiner states that the VALID + .5 signal of Kromer teaches a first sequence signal that when asserted indicates that a current instruction address is sequential to a previous instruction address even if a data address is provided between the current instruction address and the previous instruction address. However, Applicants respectfully disagree. The Examiner states that "when VALID + 0.5 is high, this signal indicates that a branch has not been encountered and the current instruction address is sequential to a previous instruction address (as shown in Fig. 2A and Fig. 2C). And this holds true even if a data address is provided between the current instruction address and the previous instruction address." However, Applicants submit that the Examiner has mischaracterized the reference. For example, VALID + 0.5 being high does not indicate that a branch has not been encountered and the current instruction address is sequential to a previous instruction address. Instead, as disclosed in col. 8, lines 4-8, of Kromer, the VALID+.5 signal is high to indicate that the current instruction is a valid instruction, i.e. one requiring decoding, and when VALID+.5 goes low, it is indicative of the fact that I_4, the jump address, is not a valid instruction, and th refore does not require

decoding. That is, the VALID+.5 signal cannot be relied upon to indicate the sequentiality of instructions, because it is instead used to indicate whether the current instruction requires decoding. Therefore, unlike the Examiner's assertions, the VALID+.5 signal is used to indicate when an instruction is a valid instruction needing decoding or not and does not indicate whether a branch has been encountered or not. For example, the branch is not actually encountered until I_N, at which point VALID+.5 remains high, even though I_N is *not* sequential to I_5 (see Fig. 2C of Kromer). Therefore, for at least these reasons, Kromer does not teach or suggest a third sequence signal as claimed in claim 18.

Claims 19-20 have not been independently addressed because they depend directly or indirectly from allowable claim 18 and are therefore also allowable for at least those reasons provided above with respect to claim 18.

Conclusion

Although Applicants may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicants are not discussing all these statements in the current Office Action, yet reserve the right to address them at a later time if necessary.

Applicant respectfully solicits allowance of the pending claims. Contact me if there are any issues regarding this communication or the current Application.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 502117.

Respectfully submitted,

By: _____
Joanna G. Chiu

Attorney of Record
Reg. No.: 43,629
Telephone: (512) 996-6839
Fax No.: (512) 996-6854

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.,
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Law Department

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